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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

NADAV, ORI

ART UNIT PAPER NUMBER

2811

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/636,466

Applicant(s)

PARK, WOON-YONG

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of a peripheral area including an upper region arranged above the display area and a lower region arranged below the display area, wherein a plurality of first and second upper repair lines formed in the upper region of the substrate, as recited in claim 1, is unclear as to how the peripheral area having an upper region located above the display area and a lower region located below the display area when the peripheral area surrounds the display area and the drawings depict the upper and lower repair lines being formed in one plane, adjacent to the display area, and not overlapping the display area.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (6,380,992).

Lee teaches in figure 7 and related text a thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate 99, 101 (figure 4b) including a display area and a peripheral area surrounding the display area, the peripheral area including an upper region arranged above the display area and a lower region arranged below the display area (figure 8);

signal lines 120, 121 (layers 121 are considered as part of the signal lines) formed on the insulating substrate, wherein the signal lines are bundled into a plurality of blocks, each block including a predetermined number of signal lines;

a plurality of first upper repair lines 220a 220b (the upper part of lines 220a, 220b) formed in the upper region of the substrate, crossing one or more of the plurality of blocks;

a plurality of second upper repair lines 220a 220b (the lower part of lines 220a, 220b) formed in the upper region of the substrate, crossing all of the signal lines (at least in that block);

a plurality of upper connection members (the vertical connections connecting the upper part of lines 220a, 220b to the lower part of lines 220a, 220b) crossing the first upper repair lines and the second upper repair lines.

Lee does not teach in the embodiment of figure 7 a plurality of first lower repair lines formed at the lower region of the substrate, connected to the corresponding first upper

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repair lines, wherein the first lower repair lines cross the signal lines crossed by the first upper repair lines;

a plurality of second lower repair lines formed at the lower region of the substrate, crossing all of the signal lines; and

a plurality of lower connection members (the block of group 131) crossing the first lower repair lines and the second lower repair lines.

Lee teaches in figure 1 the entire device wherein the lower peripheral region of the substrate is identical to the upper peripheral region of the substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use repair lines in the lower region of the substrate, identical to the upper repair lines located in the upper region of the substrate, such that a plurality of first lower repair lines formed at the lower region of the substrate, connected to the corresponding first upper repair lines, wherein the first lower repair lines cross the signal lines crossed by the first upper repair lines;

a plurality of second lower repair lines formed at the lower region of the substrate, crossing all of the signal lines (in that block); and

a plurality of lower connection members (the block of group 131) crossing the first lower repair lines and the second lower repair lines in Lee's device, in order to provide better repair capabilities to the device. Note that since the upper and lower repair lines are connected to the signal lines, then the first lower repair lines are indirectly connected to the corresponding first upper repair lines, as claimed.

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Regarding claims 2, 4 and 9, the device of Lee includes a plurality of first and second interconnection lines (signal lines) interconnecting the first upper repair lines and the first lower repair lines, wherein the first and second interconnection lines are formed on a printed circuit board.

Regarding claim 3, Lee does not teach connecting the first upper repair lines to pins. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the first upper repair lines to two or more dummy pins of integrated circuits in Lee's device in order to provide conventional external connections to the device. Note that the repair lines are linked to the first interconnection lines.

Regarding claim 5, Lee teaches in figure 7 a plurality of third upper repair lines 210a, 21b formed at the upper region of the substrate while crossing the upper connection members and all of the signal lines; and

a plurality of third lower repair lines (the lower block of repair lines 210a, 210b formed at the lower region of the substrate while crossing the lower connection members and all of the signal lines.

Regarding claim 6, Lee teaches in figure 7 that each block of the signal lines comprises the signal lines connected to an integrated circuit.

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Regarding claims 7 and 8, the device of Lee includes first upper and lower repair lines cross two blocks of the signal lines, wherein one or more of the upper and lower connection members are formed at each block of the signal lines.

Regarding claim 10, Lee does not teach using the device with a signal amplifying circuit. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the device with a signal amplifying circuit in the first and second interconnection lines in order to use the device in an application which requires a signal amplifying circuit.

Response to Arguments

Applicant argues that the claimed limitation of a peripheral area including an upper region arranged above the display area and a lower region arranged below the display area is clear, because figure 1 shows a display area 11 represented by a dashed line, and a peripheral region is represented by an area surrounding the display area 11, such that any region surrounding the display 11, which may or may not be in the same plane. Therefore, one of ordinary skill in the art would readily ascertain the metes and bounds of claim 1.

The claimed limitation of a peripheral area including an upper region arranged above the display area and a lower region arranged below the display area, wherein a plurality of first and second upper repair lines formed in the upper region of the

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substrate, as recited in claim 1, is unclear because figure 1 depicts first and second upper repair lines being formed in one plane, adjacent to the display area, and not overlapping the display area, whereas claim 1 recites first and second upper repair lines are respectively formed in an upper region located above the display area and in a lower region located below the display area.

Applicant argues that the examiner took the official notice that a plurality of lower repair lines are formed in Lee's device.

Lee teaches a plurality of upper repair lines. Claim 1 recites a plurality of upper repair lines and a plurality of lower repair lines, identical to the upper repair lines. Figure 7 of Lee depicts upper repair lines but does not depict the lower part of the display area. Figure 8 of Lee depicts repair line 140 surrounds the display area. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use repair lines in the lower region of the substrate, identical to the upper repair lines located in the upper region of the substrate, as claimed, in order to provide better repair capabilities to the device.

Applicant argues that Lee does not teach second upper repair lines crossing all of the signal lines.

Claim 1 recites signal lines are bundled into a plurality of blocks, wherein each block including a predetermined number of signal lines, and a plurality of second upper repair lines cross all of the signal lines. The broad recitation of the claim does not

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require that one repair line cross all the signal lines. Lee teaches in figure 7 a plurality of second upper repair lines 220a 220b (the lower part of lines 220a, 220b) cross all of the signal lines (at least in that block).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800

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via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.
6/3/04

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800